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SUMMARY

Professor and EET Program Coordinator with experience instructing in both the classroom and laboratory instruction. Specific expertise in C++ programming, digital design, DC circuits, and digital electronics. Demonstrated ability to adapt coursework from in-classroom to online. Effective communicator, guiding students through problem solving and debugging techniques in both classroom and online environments.

EDUCATION

Master of Science, Electrical Engineering
University of New Hampshire **Durham, NH 12/1994**

Bachelor of Science, Electrical Engineering
University of New Hampshire **Durham, NH 5/1992**

SKILLS

Design Experience

- Digital Design
- C/C++ Programming
- FPGA Design
- Schematic Capture
- VHDL
- Arduino Programming

Leadership Experience

- Creating Schedules
- Financial Management
- Fundraising
- Proposals
- Teaching
- Performance Evaluation

ACADEMIC EXPERIENCE

Nashua Community College **8/21 - present**
Professor and Program Coordinator, Electronic Engineering Technology and Computer Engineering Technology
Responsibilities include:

- EET/CET Program Coordinator
  - Instructor course/lab assignments
  - Hiring/evaluating adjunct professors as needed
  - Lead for EET ABET accreditation activities
  - Working with industry partners to establish pathways to employment

- Lecture and laboratory instruction for the following courses:

  - Digital Circuits I
  - Advanced Digital Electronics
  - Microcontrollers
  - Introduction to Programming Using C++
  - EET Capstone

New Hampshire Technical Institute **9/13 – 6/21**
Adjunct Professor, Electronic Engineering Technology
Responsibilities include:

- Lecture and laboratory instruction for Introduction to Programming with C++
- Laboratory instruction for the following courses:
  - Electric Circuits I
  - Digital Fundamentals
  - Advanced Digital Electronics
  - Integrated Circuits and Interfacing
- Lecturing on lab procedure, monitoring implementation of lab procedure, and answering questions when necessary to ensure students understand and execute the lab procedure properly
- For advanced classes, responsible for writing lab procedures, including a series of lectures and labs on FPGA design using schematic capture and VHDL in Intel/Altera Quartus Prime Lite design environment
- Grading lab reports, entering grades, and communicating with students as needed to ensure successful implementation of the lab procedures
- Collection of data and analysis of outcomes as required to support ABET accreditation of EET/CPET programs

New Hampshire Technical Institute **5/15 - present**
Lab Technician, Electronic Engineering Technology
Responsibilities include:

- Calibrating and maintaining laboratory equipment
- Selecting and procuring parts and equipment in support of EET/CPET/AGGP programs
- Mentoring students as needed with problem solving and/or debugging outside of the classroom environment
- Exploring new technologies for advanced digital electronics course applications
- Assisting in collection and organization of data for ABET accreditation of EET/CPET programs

NON-ACADEMIC EXPERIENCE

Lucent Technologies
Technical Manager, ASIC/FPGA Design **7/00 – 11/02**

- Responsibilities included staff assignments, performance review and salary administration, coordination between groups on overall staff plan and direction of ASIC/FPGA community
- Coordinating ASIC and FPGA proposal development, including schedule, cost analysis, and architecture
- Interfacing with external vendors for device manufacture and production, including negotiating schedule, process interval, model quantities, risk production device cost and liability, and model production device cost
- Supporting complete verification and validation of ASIC and FPGA devices, coordinating with hardware and software teams to ensure full test coverage

Lucent Technologies
ASIC Design **2/99-6/00**

- Block designer and lead verifier for 3 million gate Synchronous Optical Network (SONET) ASIC. Responsibilities included vendor RFQ, I/O specifications, design and verification of components, integration of transmission interfaces, device-level verification, development of